# NONDESTRUCTIVE INSPECTION TECHNIQUE OF DIELECTRIC FILMS IN METAL-OXIDE-SEMICONDACTOR STRUCTURE

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## 1. Introdaction

The charge degradation and modification of MOS-structures consisting of interface state generation and charge generation in thermal $SiO_2$ occurs under many stressing situations such as high-field charge injection, exposure to ionizing radiation, plasma treatment etc. In the present work, a new nondestructive inspection technique of multilevel current stress is proposed. This technique allows to investigate the generation of positive and negative charges, accumulating in gate dielectric of MOS structures under stressing situations. A change in the charge state of the MOS-structure is determined from the analysis of the $V_I$ time dependence. The method takes into account the process of the MOS capacitance charging by the constant current pulse. In comparison with the conventional techniques our method is nondestructive and enables to reduce the high-field stress time while measuring the injection current-voltage (I-V) characteristics of the MIS-structure. We consider this method to provide higher accuracy and to decrease the probability of dielectric breakdown. The charge degradation parameters obtained by the present method are determined before and after high-field and ionizing radiation stressing.

## 2. Technique description

Usually using the technique of the charge injection into the MOS-structure dielectric with direct current, the experimental data analysis is started after all the current flowing through the MOS-structure becomes the injection current. The processes in the MOS-structure during MOS-structure capacitance charging are normally neglected. This considerably reduces the usefulness of such a technique, as will be shown below.

The proposed injection technique consists in applying a constant current pulse to the MOS-structure and measuring the time dependent voltage, $V_1(t)$. The data analysis is carried out taking into account the MOS-structure capacitance charging. To explain the principle of the technique we shall consider the diagrams for variation of currents and voltage on the MOS-structure during the measurements (Fig. 1). The variation of $V_1(t)$ during the MOS-structure capacitance charging can be conventionally divided into the following ranges: the low-voltage and the high-voltage. The low-voltage range is considered to be a range, over which no charge is injected into the dielectric and all the current flowing through the sample is the capacitive one. In the high-voltage range, in addition to the capacitive current, there exists the current caused by charge injecting into the dielectric. The recording of the MOS-structure capacitance charging process over the low-voltage range using the constant current technique allows to test the MOS-structure parameters, which are determined, as a rule, with the C-V technique. In this case it is necessary to charge the MOS-structure by a constant current pulse with an amplitude $I_0$ (Fig. 1, a) from the mode of an accumulation or deep inversion so that the Fermi level passes over all the band gap part which is interesting for us (Fig. 1, portion 2). Then the MOS-structure capacitance time dependence can be determined with the equation:

$$C(t) = I_2 \cdot \left( \frac{dV_I(t)}{dt} \right)^{-1}, \qquad (1)$$

where t denotes the time.

Using Eq. (1) and taking into account $V_1(t)$, it is possible to determine the C-V curve which is the low-frequency C-V dependence. The requirements for the constant current pulse amplitude in

the proposed technique are similar to the requirements for the current amplitude in the quasistatic C-V technique [6].

According to Ref. 6, the surface potential $\varphi_s$ is dependent on the low-frequency capacitance C of the MOS-structure as the following:

$$\frac{d\varphi_S}{dV_I} = 1 - \frac{C}{C_i}, \quad (2)$$

where $C_i$ is the dielectric capacitance. Substituting the equation for the low-frequency capacitance (1) into Eq. (2) and integrating, one has the following expression for determining the surface potential time dependence:

$$\varphi_S(t) = V_I(t) - \frac{I_2}{C_i} \cdot t + A, \quad (3)$$

where A is the integration constant.

Thus, when charging the MOS-structure by a constant current pulse, we obtain a curve, which already is at once the integrated dependence (2). The integration constant A, as well as in the low-frequency C-V technique, is defined by the initial conditions or from other measurements. Taking into account both $\varphi_s(t)$ and $V_I(t)$, we obtain the dependence $\varphi_s(V_I)$, which allows to determine the flat band voltage. In the low-frequency C-V technique the following expression is used to determine the interface states density spectrum [6]:

$$N_{SS} = \frac{1}{q^2}\left[\frac{C(\varphi_S)\cdot C_i}{C_i - C(\varphi_S)} - C_D(\varphi_S)\right], \quad (4)$$

where q is the electron charge, $C_D$ is the theoretical differential space charge capacitance of semiconductor.

Hence, when charging the MOS-structure capacitance by a constant current pulse taking into account the equation for capacitance determination (1), the expression for defining the interface states density (4) is transformed to the following:

$$N_{SS} = \frac{1}{q^2}\left[\frac{I_2 \cdot \left(\frac{dV_I(t)}{dt}\right)^{-1} \cdot C_i}{C_i - I_2 \cdot \left(\frac{dV_I(t)}{dt}\right)^{-1}} - C_D(\varphi_S)\right] \quad (5)$$

As a result, using the constant current injection technique and taking into account the expressions (1), (3), (5) in portion I (Fig. 1, b), it is possible to determine the following dependencies: the low-frequency capacitance of the MOS-structure versus bias voltage, the surface potential versus voltage and the interface states density versus surface potential, which are usually obtained with the low-frequency C-V technique.

In portion 3 (Fig. 1, b) all the current flowing through the dielectric remains to be the capacitive one; the MOS-structure capacitance becomes to be constant and equal to the dielectric capacitance $C_i$. The dielectric capacitance measurement in this portion allows to determine the dielectric thickness when its dielectric constant is known.

Over the high-voltage range (Fig. 1, b, portion 3), when starting the charge injection into the dielectric (Fig. 1, c), the recording of the MOS-structure capacitance charging process also allows to expand the possibilities of the constant current technique [5]. Using the constant current technique in the high-field injection range the condition in which the dielectric charge variation during the high-field injection is much less than the value of the injected charge $Q_{inj}$ should be satisfied. When applying a rectangular current pulse to the studied sample it is possible to express the MOS-structure charge neutrality equation as the following:

$$Q_3 = Q_c - Q_{inj}, \quad (6)$$

where $Q_0$ is the charge supplied to the sample ($Q_3 = I_3 \cdot t$), $Q_c$ is the capacitive component of the MOS-structure charge.

Solving Eq. (6) with respect to $Q_{inj}$ and considering that an MOS-structure capacitance under the high-field injection is equal to the dielectric capacitance, one has the expression for determining the value of the charge injected into the dielectric:

$$Q_{inj}(t)=\int i_{inj}(t)\,dt=I_3\cdot t-C_i\cdot V_I(t), \qquad (7)$$

where $i_{inj}$ is the injection current. Differentiating Eq. (7) with respect to time, one has the expression for determining the injection current:

$$i_{inj}(t)=I_3-C_i\cdot\frac{dV_I(t)}{dt}. \qquad (8)$$

Measuring the time-dependence $V_I(t)$ and using Eq. (8), we determine the experimental I-V dependence for the studied sample under the high-field stress. The minimum current in the I-V dependence is limited by the measurement accuracy, and the maximum level is limited by the value of $I_3$.

The given way of measurement *I-V* of the characteristic is expedient for using in that case when it is necessary to minimize amount of the injected charge. If carry out research of change of charging characteristics of MOS-structures wider range of high-fields carry out step increase in amplitude applied current (fig. 1, portions 4..., *k*-1, *k*; where *k* - portion number on which the basic injection of a charge is made), and current-voltage characteristics receive on values of a current and voltage on each step. The quantity of steps is defined by demanded accuracy of reception *I-V* and finite value of a current at which charge injection in dielectric will be spent. Duration of a step should provide a full charge of capacity of MOS-structure and transition in a mode of injection of a charge. The equation (8) can be used also in need of expansion of a range measured *I-V* towards currents less $I_3$.

For increase of accuracy of definition of value of the injected charge it is expedient to use the following equation:

$$Q_{inj}(t)=\sum_{j=3}^{n-1}\left[I_j\cdot\Delta t_j-C_i\cdot V_{Ij}(t)\right], \qquad (9)$$

where *j* - portion number, *n* - number of portions, $\Delta t_j$ - time current an impulse on *j*-th a portion. Application of the equation (9) gives the chance to consider processes of a charge and the discharge of capacity of MOS-structure and, thereby, to raise accuracy of definition of value of the injected charge.

On *k*-th portion (fig. 1) is carried out injection in dielectric the demanded size of the charge, allowing to study processes of charging degradation of MOS-structures in high-fields. Then portion reduction of amplitude applied current is spent (fig. 1, portions *k*+1..., *n*-3, *n*-2). As a result it is possible to measure *I-V* the characteristic right after high-field stress and to receive fuller picture of charging degradation dielectric, including and influence quickly relaxing charges which flow down after removal current stress.

On *n*-1 portion (fig. 1) polarity current stress change on opposite and the MOS-structure recharge begins. On *n*-1 portion (fig. 1) where through MOS-structure injection and capacitor currents simultaneously proceed, dividing them by a technique [5] and having taken advantage of the equation (8), having replaced $I_3$ on $I_{n-1}$, also it is possible to calculate *I-V* the characteristic in a range of currents more low $I_{n-2}$.

On *n*-th portion (fig. 1) the injection current becomes equal to zero, and in this case *n*-th portion on dependence $V_I(t)$ appears is equivalent to 2-th portion. Then, using equations (1, 3, 5) and having replaced in them $I_2$ on $I_n$, on *n*-th portion, also it is possible to calculate low-frequency *C-V* dependence and to define MOS-structure parameters right after high-fields injections.

Such way of reception *C-V* and *I-V* characteristics, within the limits of the same technique, allows to determine characteristics of charging degradation right after tunnel injection, having lowered influence relaxation processes. The subsequent realization of the offered algorithm at opposite polarity applied current allows to determine density charge, capture cross-sections of charging traps and centroid a charge in dielectric films.

Having received experimental the current-voltage characteristic, we choose the corresponding theoretical model of electron transport. Thus, for thermal $SiO_2$ films the transport under high-fields, as a rule, by the Fowler-Nordheim model, theoretical expression for current density in which according to [7] looks like:

$$J = A\frac{V_I^2}{d_{ox}}\exp\left[-\frac{Bd_{ox}}{V_I}\right], \tag{10}$$

where $d_{ox}$ - a thickness dielectric, measured in sm, and members $A$ and $B$ it is possible to present as

$$A = \frac{q^3 m_o}{16\pi^2\hbar m^* \varphi_B} = 1{,}54\cdot 10^{-6}\cdot\frac{m_o}{m^*}\frac{1}{\varphi_B} \tag{11}$$

$$B = \frac{4}{3}\frac{(m^*)^{1/2}}{q\hbar}\varphi_B^{3/2} = 6{,}83\cdot 10^{-7}\cdot\left[\frac{m^*}{m_o}\right]^{1/2}\cdot\varphi_B \ , \tag{12}$$

where $q$ – charge of the electron; $\hbar$ - Planck's resulted constant; $\varphi_B$ - height of a potential barrier on injecting interface, measured in eV; $m_0$ - weight of electron in vacuum; $m^*$ - effective weight of electron in $SiO_2$.

Having received experimental current-voltage characteristic in Fowler-Nordheim coordinates $\lg(Jd_{ox}/V_I)$-$d_{ox}/V_I$, considering (10□12), it is possible to define such important electrophysical characteristic MOS-structure, as value of a potential barrier on injecting interface $\varphi_B$ and effective weight of electron m* in film $SiO_2$. On the other hand, at use of the given technique in the conditions of manufacture when the test is carried out on the MOS-structures made on one technology, and one of parameters $\varphi_B$ or $m^*$, or both together, the control of a thickness of oxide $d_{ox}$ which is the important technological parameter is a priori known, possible. On the found values of capacity of MOS-structure, with the account of its geometrical sizes, dielectric constant of oxide is determined.

Nowadays, the constant current stress technique [1, 5] is widely used for investigation of positive charge generation in MOS structures. In this technique, a constant current pulse is applied to a MOS structure, causing the charging of structure capacitance and initiating the mode of Fowler-Nordheim high-field tunnel electron injection. Measuring the MOS structure voltage shift one can estimate the charge state change of a sample [1, 5].

However, under high densities of tunnel current, the positive charge generation rate increases. Hence, when an injection current begins to flow in a gate dielectric, it can generate a part of positive charge, not taking into account in this technique. As a result, the constant current technique at high densities of injection current can give underestimated values of positive charge. The usage of other techniques of positive charge value determining, for example C-V technique or charge pumping, requires the interruption of injection and the re-commutation sample. It can lead to relaxation of a part of the positive charge and significant errors in its determination.

To eliminate this shortcoming, a special algorithm to control the current stress applied to a sample was proposed, shown on Fig. 1(a). Two levels of current are applied to the structure: stress level $I_S$ and measuring level $I_m$. Positive charge generation in the gate dielectric is caused by stress current value $I_S$. The current $I_m$ must have a value of several orders less than $I_S$, to minimize the dielectric charge degradation by this current. The MOS charge state change can be estimated by the voltage shift on MOS structure at current $I_m$ (Fig. 1b). Voltage shift under current $I_m$ takes into account positive charge generated in the gate dielectric right after the switching to the current $I_s$. Thus, the inherent errors of constant current technique are reduced when utilizing our technique.

For investigation of positive charge generation, the pulse short-time change of current level from $I_s$ to $I_m$ and vice versa can be used (Fig. 1). The stress mode duration $t_s$ depends on the monitoring discreteness of positive charge, it can be varied on different stages of injection. The measuring mode duration $t_m$ must provide the establishing of injection mode, but it should not affect significantly on the sample charge state.

## 3. Example

Let us consider how the present method is implemented in portions I and III shown by fig.1. The MIS capacitors made on commercially available phosphorus-doped (resistivity 4.5 Ω·cm) Si <100> wafers were used as the test samples. Silicon dioxide of thickness 7÷100 nm was thermally grown in $O_2$ at 1000°C with an addition of 3% HCl. Then aluminium films 1.2 μm thick were magnetron-sputtered. At the next process stage, Al electrodes of the area $1.5x10^{-2}$ $cm^{-2}$ were photolithographically formed, and the oxide on the back wafer side was removed. Subsequent annealing was performed at 475°C in nitrogen.

The measurements were performed by means of special experimental setup consisting of:

- a specially designed current source allowing to control the current pulse level of $10^{-10} – 10^{-2}$ A by the program;
- a voltmeter for measuring the variation of the voltage across the MIS-structure;
- a computer (IBM Pentium) controlling the setup and analyzing the experimental data.

First, the studied structure was charged to the voltage of –5V. After that the positive dc pulse with the amplitude of $10^{-10}$A corresponding to the current density of $J_0=5\times10^{-9}$A/cm$^2$ was applied to the structure. The time dependence of the voltage applied to the sample is shown in Fig.2. Then using Eq. (3) we determined the surface potential variation as a function of the bias voltage. Fig.3 shows the low-voltage capacitance of the MIS structure versus the bias voltage. Solid line is the C-V characteristic measured by the quasistatic technique. Triangles show the C-V dependence calculated with Eq. (1) from the experimental curve of Fig.2. As shown in Fig.2, the present method gave identical results to the quasistatic technique. A small difference appeared only in the C-V dependence portions related to the silicon band gap edges and were characterized by small capacitance variation. Then using Eq. (3) and (5) we were able to calculate the interface states density spectrum. The interface states density spectrum calculated with the present method and with the quasistatic technique are fully equivalent. They differ only in the ranges close to the band gap edges, according to the C-V dependences shown in Fig.2.

When voltage applied to the MIS structure reached the high-voltage range, the injection current started flowing through the dielectric (Fig. 1, c). In this portion we calculated the injection current time dependence with Eq. (8). Then taking into account the time dependence $V_1(t)$ we plotted the MIS structure I-V curve. The MIS structure I-V characteristic in the Fowler-Nordheim representation is shown with triangles in Fig.4, solid lines are the theoretical I-V curves, squares are the I-V curve measured by the ramp technique [8]. From Fig.4 it can be seen that in the range of the low currents and when approaching the value of $I_0$ the I-V curve obtained with the injection technique deviates from the I-V curve obtained by the ramp technique. This was caused by the measurement accuracy since the derivative $\partial V_1(t)/\partial t$ variation was insignificant in these portions. The realization of the proposed method using the given experimental setup allowed to obtain the I-V characteristics within the current variation of one order and a half.

## 4. Conclusions

1. The injection technique for testing and studying the charge degradation in metal-insulator-semiconductor structures has been proposed. This technique allows to:

- measure change in the charge state of the MIS structures and to produce charge injection into dielectric using the same technique;
- evaluate the effective charge of dielectric, the interface state density, the flat band voltage, the surface potential value for a given bias, the potential barrier height on the injection interface, the dielectric capacitance;
- determine the variations of the voltage depended on the injected charge, the concentration of the charge traps and their capture cross-sections, the value of the charge injected into dielectric until the sample breakdown occurs as well as to locate the charge centroid in dielectric.

2. A new technique for investigation of positive charge generation in gate dioxide of MOS structure under tunnel Fowler-Nordheim injection from silicon was proposed. The technique is based on the current stress controlling, applied to the sample and simultaneous voltage measurement. In this technique, the stress current level is used to generate the positive charge, and the measuring current level is used to monitor the charge state change of a sample. The proposed technique allows carrying out the controlled electron injection into gate dielectric at high-fields, realizing the simultaneous monitoring of MOS structures charge state change both under the present field and under lower fields, that gives possibility to obtain new information about charge generation processes in dielectric layers. Right after high-field injection without sample re-switching, the technique allows, to monitor the positive charge generation in the gate dielectric of MOS structures in wide range of electric fields.

**References**


1. Nissan-Cohen Y., Shappir J., Frohman-Bentchkowsky D. J.Appl.Phys., 1985, v.57, № 8, p.2830-2839.
2. Fischetti M.V. J.Appl.Phys., 1985, v.57, № 8, p.2860-2879.
3. Holand S., Hu S. J.Electrochem.Soc., 1986, v.133, № 8, p.1705-1712.
4. DiMaria D.J., Cartier E., Buchanan D.A. Anode hole injection and trapping in silicon dioxide// J. Appl. Phys. 1996. Vol.80. № 1. P.304-317.
5. Bondarenko G.G., Andreev V.V., Loskutov S.A., Stolyarov A.A. The method of the MIS structure interface analysis // Surface and Interface Analysis. 1999. V.28. P.142-145.
6. Castagne R., Vapaille A. Surface Sci., 1971, v.28, p.157-193.
7. Weinberg Z.A. J.Appl. Phys., 1982, v.53, № 7, p.5052-5056.
8. Arnold D., Cartier E., DiMaria D.J. Theory of high-field electron transport and impact ionization in silicon dioxide// Phys. Rev. B. 1994. Vol.49. № 15. P.10278-10297.
9. Green M. L., Gusev E. P., Degraeve R., Garfunkel E. L. Ultrathin (<4 nm) $SiO_2$ and Si–O–N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits // J. Appl. Phys. 2001. Vol.90. No.5. P.2057-2121.
10. Al-kofahi I. S., Zhang J. F., Groeseneken G. Continuing degradation of the $SiO_2$ /Si interface after hot hole stress// J. Appl. Phys. 1997. Vol.81. № 6. P.2686-2692.
11. Bondarenko G.G., Andreev V.V., Stolyarov A.A., Tkachenko A.L. Modification of metal-oxide-semiconductor devices by electron injection in high-fields// Vacuum. 2002. Vol. 67/3-4. P.507-511.
12. Andreev V.V., Baryshev V.G., Bondarenko G.G., Stolyarov A.A. Multilevel-Injection Characterization of Positive-Charge Generation and Relaxation in MOS Oxide // Russian Microelectronics, 2003. T.32. № 2. P.119.
13. Bondarenko G.G., Andreev V.V., Maslovsky V.M., Stolyarov A.A., Drach V.E. Plasma and injection modification of gate dielectric in MOS structures// Thin solid films. 2003. V.427. P.377-380.
14 Bondarenko G.G., Andreev V.V., Drach V.E., Loskutov S.A., Stolyarov M.A. Study of temperature dependence of positive charge generation in thin dielectric film of MOS structure under high-fields // Thin solid films. 2006 V.515. 670-673.

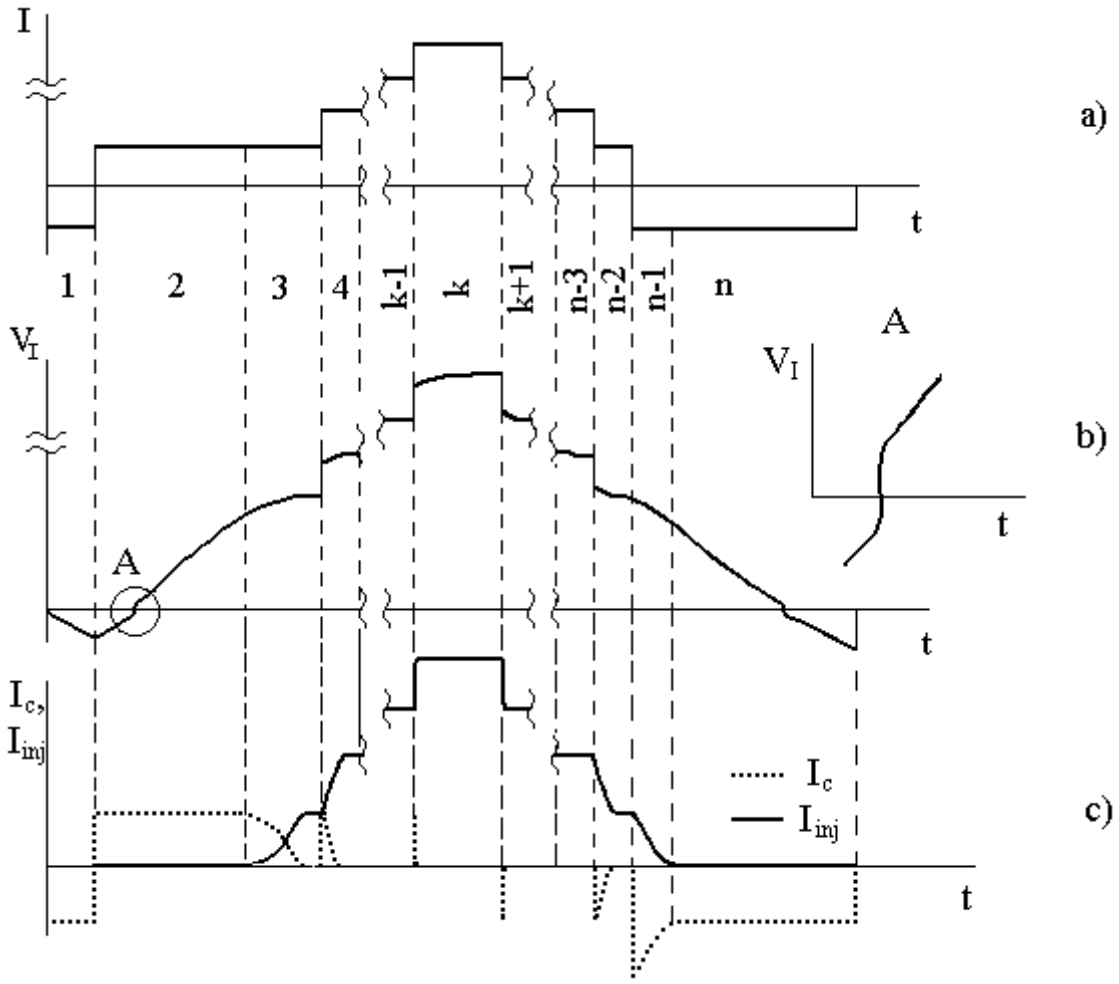


**Fig.1.** The time dependences of the values corresponding to: the amplitude of the current pulse applied to the MOS-structure (a), the measuring voltage on the MOS-structure (b), the capacitance and injection current flowing through the MOS-structure (c). A - The time dependence of the voltage changes on the MOS-structure corresponding to portion 2.

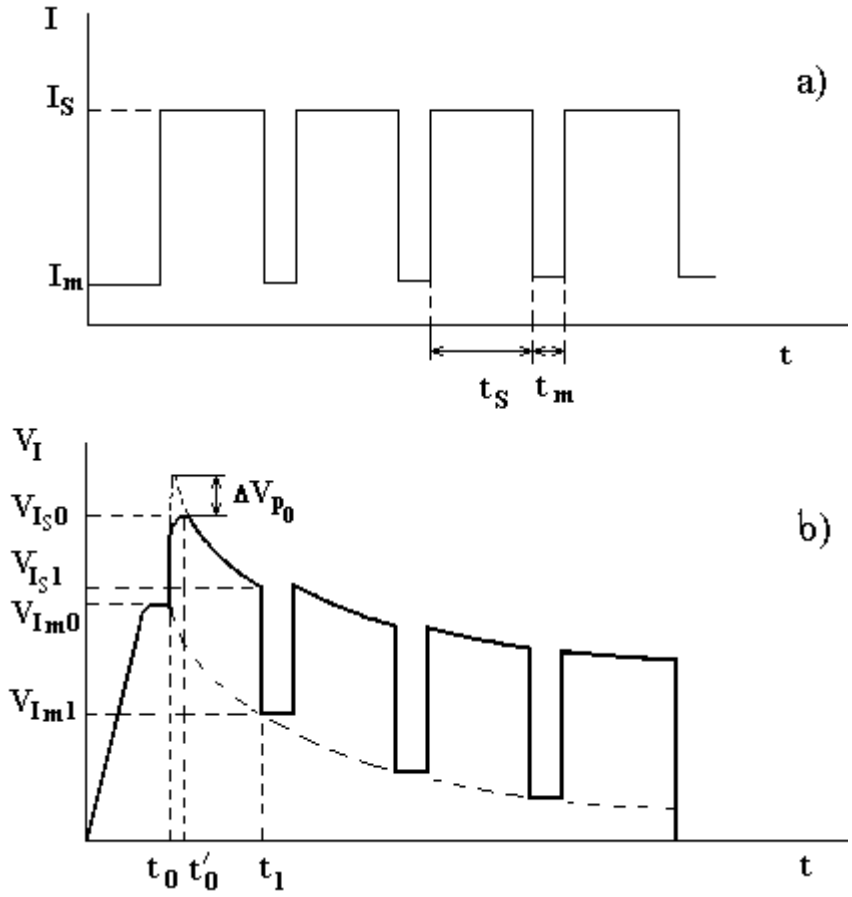


**Fig. 2.** Time dependence of current stress (a) and high-voltage part of MOS structure voltage, (b) for multilevel current stress technique.

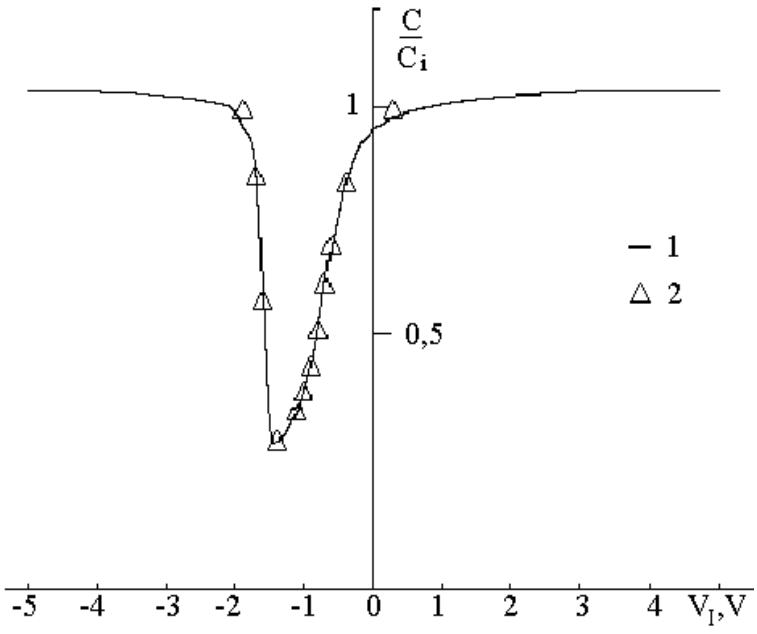


**Fig.3.** The C-V characteristics obtained with the following techniques: the quasistatic technique (1), the constant current technique (2).

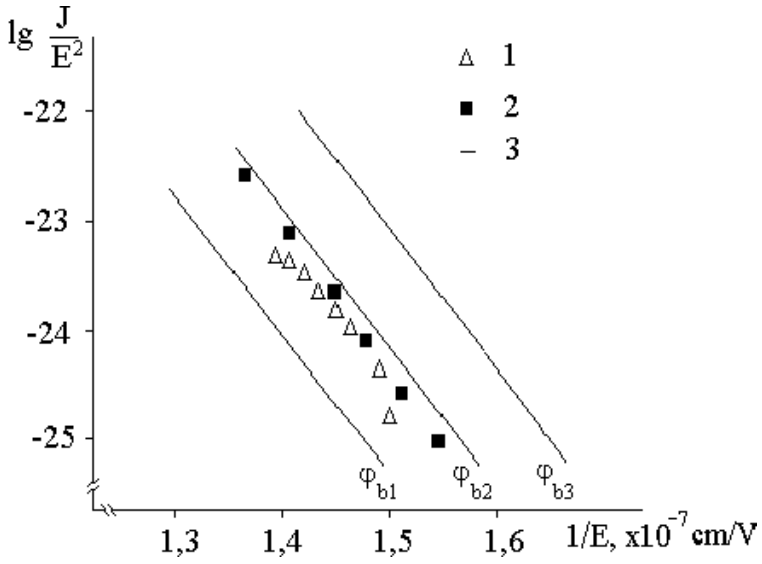


**Fig.4.** Fowler-Nordheim plots of tunneling data from the constant current injection technique (1); the linear voltage scanning technique (2); the theoretical I-V curves for the different values of the potential barrier height (3), $\varphi_{b1}$=3.3 eV, $\varphi_{b2}$=3.2 eV, $\varphi_{b3}$=3.1 eV.