4.3.18. COMPLEX APPROACH TO SOLUTIONS OF FAILURE ANALYZE SUBMICRON SEMICONDUCTOR DEVICES

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Development of modern equipment unable to imagine without using complex electronic component base which develops the same time too. Modern integral microcircuit consist of big number of elements on chip (up to several millions transistors per chip), which sizes each year becomes less (nowadays topology norm of modern BIC is less then 50 nm). Reliability and failure resistant of modern equipment in main part depend on reliability of electronic elements base. Methods of implementation for reliability determination and failure detection of using electronic components are known. Developers of electronic components test their devices, during which they detect failures. The next stage is failure analyze. Unfortunately, not all electronic factories have equipment for failure analyze. Even if they have it – it is a single devices, that don't let to make complex research and to detect true reason of failure. Creating of such laboratories limits by high cost of equipment and absence of qualified personal.

In the year 2007 in Moscow Institute of Radio Engineering, Electronic and Automatic (technical university) on the base of Laboratory of Non-destructing Control Equipment were created educational and on-the-job training center by creating nanomaterials and nanodiagnostics of microchip devices (NanoCenter of MIREA).

On of the task of Center is failure analyze of microchip devices.

Methodologies and technological route of failure analyze were developed.

1. Primary information analyze about type of failure by the data of device functional tests (carry out by Customer).
2. Electric measurements (input and output volt-amper characteristics of circuits, power circuits) to detect critical changes in characteristics. Tests on AWP of IC electric control.
3. High resolution digital X-Ray television and digital tomography synthesis of devices for identification of sealing scheme and its quality, constructive features, chip size, analyze of IC construction, bonding pad location, detecting cavities and additional elements in case. Uses AWP of X-Ray high resolution IC control.
4. IC case encapsulation for next analyze of assembling quality. Uses AWP of mechanical and chemical preparation without failures in IC functionality.
5. Optical control of IC view to control quality of encapsulation case and primary analyze of IC constructing features. Uses AWP of optical control.
6. Analyze of IC thermo map with localization overheating and "cold" zones (detecting short-cut and open-circuit). Uses AWP of Infrared Microscopy.
7. Panoramic photographing IC upper layer for documentation IC constructive fea-tures. Uses AWP of optical topological chip analyze with special software for editing digital optic images, combination and superposition topology parts of separate functional units.
8. Operation of chemical-mechanical preparation for extracting chip or chips out of case. The task of this operation is getting access to chip. Uses AWP of mechanical and chemical IC preparation.
9. Preparation IC topology for isolation researching unit from scheme for detailed

electric characteristic analyze of failure unit. Uses AWP of IC nanosize preparation and probe testing based on Helios NanoLab.

10. Electric measurements of changes in characteristics and compare with model characteristics for researching unit. Uses AWP of IC nanosize preparation and probe testing based on Helios NanoLab.

11. Operation of Plasma-Ion-etching upper layer of dielectric isolation for getting access to upper metallization layer. Uses AWP of RIE per-layer preparation.

12. Operation of chemical etching metallization layer. Uses AWP of mechanical and chemical IC preparation.

13. Panoramic photographing of topology layer. Uses AWP of optical topological chip analyze.

14. Making cross-section in the places of supposed failure with visualization of primary failure sign (high-resolution scanning electronic microscopy, transmission scanning electronic microscopy, element microanalyze). Uses AWP of IC nanosize preparation and probe testing based on Helios NanoLab.

Thereby, in educational and on-the-job training center by creating nanomaterials and nanodiagnostic microchip devices (NanoCenter MIREA) was compactly collected complex of equipment, that let make complex failure analyze microelectronic devices and establish failure reason.